Development of an IEC test for crystalline silicon modules to qualify their resistance to system voltage stress

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ABSTRACT

IEC 62804 Ed. 1, \textit{System voltage durability qualification test for crystalline silicon modules}, is being developed. First, two module designs are compared in chamber and in the natural environment of Florida (USA). From these results, a stress level of 60 °C, 85\% relative humidity, a bias of nameplate system voltage, 96 h dwell, and a pass/fail limit of 5\% relative power degradation at 25 °C and 1000 W/m\textsuperscript{2} irradiance is initially proposed for the draft protocol. This paper next focuses on one of the main controversies within the development of this standard—the use of damp heat in an environmental chamber versus a conductive foil to complete the circuit to ground during the test. Conventional 60-cell multicrystalline silicon modules with (i) a standard aluminum frame, (ii) a modified frame, and (iii) a rear rail design were tested for potential-induced degradation (PID). These three module designs were stressed at the draft protocol conditions stated above and outdoors, applying negative system voltage bias during hours of daylight to simulate array voltage. The damp heat environmental chamber tests run according to the protocol distinguish the relative resistance of five module designs to PID in the field and correctly rank-order the durability in the field to the extent tested (up to 28 months). Finally, the degradation rate is determined at 25 °C using a foil to ground the module face on a subset of modules susceptible to PID, and the results with respect to measured field performance of the modules are discussed. Copyright © 2013 John Wiley & Sons, Ltd.

KEYWORDS

Energy conversion; Silicon

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Received 28 June 2013; Revised 5 September 2013; Accepted 18 September 2013

1. INTRODUCTION

Mechanisms including polarization [1] and potential-induced degradation (PID) [2] have been found to be responsible for rapid and severe degradation of power output of some crystalline silicon (c-Si) solar photovoltaic (PV) modules. The c-Si terrestrial design and qualification test, IEC 61215 Ed. 2 [3], does not examine the stresses that elevated system voltage exerts on modules in the natural environment over time, which can degrade the power output. There are hence numerous requests for a recognized standard for evaluating system voltage durability, where the levels of stresses that are applied give an expectation of durability in the natural environments of concern to the market, without needlessly over stressing them. This paper first introduces some key experimental results toward this goal and an IEC qualification test for system voltage durability, IEC 62804 Ed. 1. The focus then turns to what has been one of the principal controversies within the development of this IEC test—using humidity at elevated temperature within an environmental chamber versus using a foil (or similar) conductor over the faces of the module to simulate the grounding of the module faces that occurs to some extent in the natural environment.

For chamber tests, the level of stress applied is typically 85 °C with 85\% relative humidity (RH), carrying over from the IEC 61215 Ed. 2 damp heat stress test, modified by the addition of system voltage bias [4–6]. Temperature was however lowered considering results that silicon nitride in some modules was found to degrade in tests of 6 days duration at 70 °C, 70\% RH, and −1000 V bias, and series resistance losses due to corrosion were found in tests of similar duration at 85 °C, 85\% RH that are suspected to not be representative of field failure [7]. It has been found that the level of 85 °C, 85\% RH, −1000 V
leads to degradation in only 44 h in p-type Si modules that is completely irreversible by thermal activation, whereas it is generally believed that PID in the field is mostly recoverable [8]. In an effort to replicate the nature of the degradation that is understood to occur in the field, the temperature in the 85% RH environmental chamber was specified to be 60 °C for the system voltage durability standard under development. At this writing, the test stipulates application of the module nameplate rated system voltage to the active cell circuit, two modules for each polarity, and 60 °C, 85% RH environmental chamber conditions for a 96 h dwell.

While the mechanisms for system voltage degradation are still being clarified, it is understood that ionic transport occurs through the glass and encapsulant, and those ions are involved in the degradation itself. The ionic species candidate is the sodium ion present because of the 13–14 weight percent NaO2 that is a constituent of the soda lime glass module superstrate used to lower the glass melting point and thus the cost. Such positive ions have been discussed as creating electric fields in the antireflective coating or passivation layer [9]. Sodium has also been found in high concentrations in stacking faults penetrating the junction [10]. It has also been speculated that ions accelerated over an insulating dielectric or antireflective coating under an electric field may imbed in and damage the junction [11]. Corona discharge over cells has been found to induce PID-like junction failure [12]. Considering that both reversible and irreversible components of junction failure are observed to be associated with system voltage stress [8], it is conceivable that multiple mechanisms are active.

An important element in the electrical circuit from the high voltage biased active layer (cells) of the module to ground with respect to PID is the extent to which the module glass surfaces provide the conduction path to ground. Current flow on glass surface is promoted with humidity and temperature, and alkali ions may migrate to the surface (leach) with time [13]. Dew on the surface of a module and rain showers are especially effective in elevating leakage current [14,15]. While PID is observed in humid climates, it is also found to occur extensively in the warm Mediterranean climates of southern Europe, so the effect of temperature must also be considered [16]. In an environmental chamber, surface conductivity is increased by increasing RH associated with adsorption of water molecules. The resulting thin water film has increasing conductivity with increasing temperature. Current transport through the superstrate is also controlled by the conductivity of the materials. Soda lime glass with NaO2 concentrations typical of solar glass can have resistivity in the range 10^{10} Ohm·cm at temperatures relevant to fielded modules [17]. Humidity may diffuse into or out of the encapsulant, also affecting ion motion within; the extent depends on the module materials, cell geometry (consider the multiple holes in metallization wrap-through cells), and environment. Factors such as these influence the motion of ions to or from the cells. Leakage current of various module package assemblies as a function of encapsulant and superstrate at varying temperature and RH has been shown, and higher leakage current and degradation rate are found with higher temperature and humidity [7,18,19]. While relationships between degradation and leakage current can be made and ion transport mechanisms can be used to explain them, there are many extenuating parameters that make generalized relationships between leakage current and degradation very difficult—ionic current must proceed to the cell dielectric (anti reflective coating) or semiconductor, not grid fingers, not metal tabs or ribbons, and not through pinholes or porosity in the backsheet to the back surface metallization. A more conductive antireflective coating on cells can reduce the resistive pathways to the semiconductor, but it will also typically reduce PID [2].

In addition to chamber tests using temperature and humidity to achieve grounding on the module, there are many examples of methods using conductors (e.g., conducting fluids, pastes, or metal foils) placed on the module face [20]. If a uniform and consistent contact with the module surfaces is made, the grounding would extend the entire face of the module, independent of module size, frame design, and the resistive path between any grounded mounting points and the module surfaces, unlike in the natural environment. Such grounding with foils has frequently been used for screening tests for PID due to its perceived simplicity. However, understanding of foils is incomplete, including the extent to which textured glass surfaces can be contacted, the criticality of achieving uniform contact to glass surfaces, acceptable RH limits considering possible humidity interactions with the glass and encapsulant, acceptable temperatures for test such that the PID processes that are observed in the field are replicated, and acceleration factors as a function of temperature with respect to degradation in the natural environment so that meaningful stress levels and durations can be determined. In this work, we comparatively examine the rate of degradation for two replicas of one module design tested in chamber and outdoors with the rate under Al foil to get information about what previously proposed durations of this test (e.g., 168 h [20]) actually mean about the reliability of the modules that pass it within the 5% degradation limit.

In accelerated lifetime studies of thin-film modules, it was found that rear support rails or mounting posts bonded to the back surface of modules slow degradation because of the increased resistance in the circuit from the active layer to ground [21]. Use of rear rails, mounting posts, or limited glass contact area mounting clamps has become quite prevalent for thin-film module designs, and some c-Si manufacturers have also adopted these designs. Wrapping a module in a conductive foil over the glass, frame, and mounting points short-circuits the benefits of this design that was found to make the module more durable in chamber; however, it has not yet been shown to what extent the minimization of frame contact to the glass provides in terms of durability to system voltage stress in the natural environment. In addition to
clarifying this, we seek to determine how well the damp heat chamber tests represent the rate of PID in the natural environment for c-Si modules with various frame designs. While there have recently been many excellent efforts to develop equations to predict the rate of PID, this paper focuses on experimentally determined factors for acceleration and checking that the module designs that pass the proposed system voltage durability qualification test stress levels are indeed stable to PID in the natural environment.

2. EXPERIMENT

Conventional 60-cell Si (n+ p front junction) modules with Al frames were modified to make two additional designs: one with a metal frame only on the two short (~1 m) lengths of the module, and another design with fiberglass rear support rails and no metal frame. The original and the two modified designs were tested for PID in multiple replicas in chamber tests at 60 °C with 85% RH, and module nameplate system voltage in negative bias (~1000 V) was applied to the shorted module leads. The metal frame or frame segments were ground-connected. In the case of the modules with rear rails only, four mounting points on the fiberglass rails were grounded. In all cases, precautions were taken to ensure any leakage current flowed through the intended grounding points. Additional conventional framed multicrystalline (mc-Si) module designs (referred to as type 1 and type 2) were tested at 60 °C and 85 °C with 85% RH and ~600 V nameplate system voltage bias applied for understanding of the temperature-dependent acceleration and for comparison to modules of these two types mounted outdoors. Module power ($P_{\text{max}}$) monitoring during the accelerated lifetime testing was achieved using the previously described technique of superposition with dark current–voltage ($I$–$V$) curves obtained in situ in the chamber [7]. $P_{\text{max}}$ of the modules was also measured less frequently with a solar simulator during the stress testing, and the correspondence with the dark $I$–$V$-derived $P_{\text{max}}$ values was verified. Failure points examined for acceleration factor determination are 5% loss in standard test conditions (STC) power, corresponding to proposed IEC 62804 Ed. 1 committee draft qualification test limit, and 20% loss in STC power, a common warranty limit for modules.

Replicas of the previously discussed module designs (including those with modified frames) were placed in the natural environment, also applying nameplate system voltage in negative bias during hours of sunlight to simulate array voltage. The modules were located in Florida, USA, a hot, humid, subtropical environment near the Atlantic Ocean coast. They were placed horizontally to replicate a flat roof-mounting scenario. More information about the system can be found in [7]. Salt mist and some water pooling on the modules after rains provide conductive paths from the module face to ground for extended periods and provide for a relatively stressful natural environment for understanding the limitations of these modules’ resistance to PID. Individual modules self-biased (positive) to their maximum power point were similarly placed outdoors to understand any other degradation behavior that might be occurring simultaneous to PID. Depending on the module, $P_{\text{max}}$ of the modules was either measured periodically on a flash tester after dismounting the module or directly on the mounted module with an $I$–$V$ tracer using a DC electronic load, in which case the measured curves were adjusted to STC power. Power values in this work are reported as a ratio to their initial power taken after a 5 kW/m² light soak to remove effects of any light-induced degradation from the analysis. Triggering of the $I$–$V$ curve traces of the mounted modules was performed automatically with a switching network during stable plane-of-array irradiance conditions between 200 and 350 W/m² for the understanding of low-light behavior effects of PID and between 700 and 1000 W/m². The module current itself was used to normalize the effect of irradiance under varying spectral conditions to calculate the irradiance-adjusted $I$–$V$ curve. Gamma factor ($\gamma = 1/P_\text{STC} \cdot \frac{dP}{dT}$, where $P_\text{STC}$ is the module power at $T = 0 \degree C$) correction for maximum power as a function of temperature was then factored to estimate the 25 °C power. Module gamma factor change as a function of time and degradation was checked out of concern that the temperature-dependent module performance may also be degrading with PID. The underlying method used by Smith and coworkers for degradation rate determination [22] was applied, whereby the $\gamma$ factor leading to the minimum standard deviation in STC-adjusted power calculated for numerous $I$–$V$ curves of a fielded module taken at various temperatures in a segment of time is chosen. The most stable readings of the $\gamma$ factor at ~0.00465 were determined, and no clear trend in degradation (increased temperature sensitivity) of $\gamma$ was observed. This value, close to the manufacturer’s specified value, was therefore applied to calculate STC power from the irradiance-corrected $I$–$V$ curves.

Tests with Al foil on the module face were performed at 25 °C and 40% RH. A rubber mat was used to apply weight on the Al foil so that the foil contact to the glass of the horizontal module would remain constant throughout the test. Nameplate system voltage (~1000 V) was applied to the shorted module leads.

3. RESULTS AND DISCUSSION

In the following sections, we first discuss (i) the experimental results of two conventional framed mc-Si module designs (types 1 and 2) that form the initial basis for the stress levels considered in the system voltage durability standard under discussion. This is followed with (ii) the results and discussion of mc-Si modules with modified frame designs to further examine the appropriateness of the standardized test stress levels and the ability of the accelerated test to predict the durability of the modules to
system voltage effects in the natural environment. Finally, (iii) two replicas of this module laminate were stress-tested for PID with Al foil (using its supplied Al frame) to obtain comparative data. Some considerations for future developments in testing for system voltage durability are discussed.

3.1. Choice of stress factors and levels

The 96 h duration specified in the committee draft of IEC 62804 Ed. 1 originates from a module design that degraded 5% in 96 h time at 60 °C, 85% RH, and −600 V, indicated as module type 1 in Figure 1. This module was also monitored in two replicas in the Florida environment and appears to be stable in the −600 V system voltage bias configuration for over 28 months, indicated as module type 1 in Figure 2. Module type 1 is considered, for the purpose of a qualification test for PID, to have satisfactory performance at this time. On the other hand, the second module design (type 2) with performance data shown in Figures 1 and 2 proved not to be resistant to PID. These modules failed at the 5% relative power loss criterion on the order of a day in test at the 60 °C, 85% RH, −600 V stress level. The first replicas of module type 2 degraded 5% in around 200 days in the outdoor test. For comparison, one of each of these module types that were placed on a maximum power point tracking device, self-biased to the individual modules’ maximum power point voltage (positive with respect to ground) and also periodically flash-tested, displayed relative power changes at month 28 (this writing) of 1.4% and 2.1% lower than the initial readings for type 1 and 2, respectively (Figure 2). The relative power reductions of the two replicas of module type 1 under −600 V bias are 1.7% and 2.2%, and must be considered insignificantly different than the losses in the self-biased modules. Handling of these modules for frequent flash testing may have contributed to the observed degradation.

One additional replica of module type 1 was placed under −1500 V bias during daylight hours at the outdoor test site, almost twice the nameplate rated system voltage, to understand the relative effect. It is seen in Figure 2 that this module shows up to 8% relative degradation at month 19 (July 2012) followed by a recovery in power. This evidence of modest degradation in the over-biased module tells us that the level of stress applied in the proposed draft standard is not forcing overdesign.

Effects of seasonality are also evident in Figure 2. Exceptionally rapid degradation is seen in the hot late-summer months (July through September), especially in year 2. However, subsequent partial recovery in the winter months can also be observed. A plot of coulombs (daily and accumulated) versus date for type 2 modules (Figure 3) shows elevated leakage current in the summer months and reduced leakage current in the winter months. As discussed previously, relationships between increased temperature, RH, and surface wetness and increasing module leakage current are well documented. This plot however shows evidence of a net rate of ion approach to the biased active cell circuit in the module that must be exceeded for degradation to occur. Below this level, there is net positive ion motion toward the active cell circuit occurring simultaneously with recovery in power. Leakage current, when

Figure 1. Chamber testing of conventional (n⁺/p) multicrystalline silicon module replicas at 85% relative humidity and nameplate rated system voltage (−600 V) applied to the cell circuit at temperatures shown. At the 60 °C proposed test condition, module type 1 degrades 5% relative in approximately 96 h.

Figure 2. Outdoor potential-induced degradation data for two module designs under −600 V system voltage bias during hours of daylight. The colored data points correspond to different replicas. Two replicas of module type 1, a design previously found to degrade about 5% in 96 h in chamber at 60 °C, 85% RH, appear stable, as does a self-biased control after 28 months. One replica of module type 1 was also stressed outdoors at −1500 V bias, where some degradation was observed. Type 2, not stable in the accelerated test, is also seen here to rapidly degrade in the outdoor environment. Notice there are two differing start dates for the outdoor testing of type 2 modules. Evidence of seasonality in the degradation and recovery can be seen. The lines connecting the data points are drawn to guide the eye.
modeled linearly for simplification. We previously found that the power drop could be
attributed to two replicas for each design tested. The rate of module degradation with the two-edge frame is
slowed compared with that of the full-framed module; the ratio of the degradation rate is 0.51 (P < 0.001),
and it was successfully reproduced here. The effects of system voltage stress depend on numerous
elements of the leakage current pathways from the active cell circuit to ground; one component being varied in
industry is the module frame and mounting point design. The relationships between the environmental chamber
tests and the outdoor tests for the modules with varying frame designs are summarized in Table I. The ratios
of the 96 h (4 days) required to pass the proposed qualification test. We caution that the rate of degradation of
these framed modules is quick; thus, uncertainty exists in the exact time of the 5% degradation point. The modules
with the fiberglass rear rails were tested beyond what is shown and found not to degrade at all. It is thus seen that the environmental chamber stress test for PID differentiates and ranks the durability of the three
designs in accordance with the anticipated efficiency of charge transfer from the glass face to ground.

3.2. Potential-induced degradation as a function of frame design

The relationships between the environmental chamber tests and the outdoor tests for the modules with varying frame designs are summarized in Table I. The ratios between time to failure outdoors and time to failure in the chamber stress tests are computed considering failure for 5% degradation ($0.95 \times P_{max,0}$) and for 20% degradation ($0.80 \times P_{max,0}$). These acceleration factors in time or in coulomb charge transferred are simply field-to-chamber test ratios, with no presumption of accounting for the inherent variability in the field stress levels. While it must be cautioned that seasonality strongly influences the degradation curves, we must nevertheless examine this data to understand the scale of the acceleration. The mean ratios for the 5% degradation criterion for the framed and two-

Figure 3. Daily and cumulative coulombs leaked over the period for type 2 module mounted outdoors with −600 V bias applied during daylight hours. There are four replicas indicated by points of different color. Note also the different test periods. The elevated charge transfer to the −600 V (daytime) biased cell circuit during the summer months is evidence of seasonality.

Figure 4. Degradation in maximum power normalized to the initial maximum power as obtained by chamber in situ dark I–V measurements for three module designs as shown (two replicas each) as a function of time. The stress levels in the environmental chamber are 60 °C, 85% RH, and −1000 V. The data is fit linearly with the time (days) scaled to the power of two. The inset shows the relationship between the normalized maximum power determined in situ showing good correspondence to values obtained at less frequent intervals with a solar simulator.
edge framed modules (200 and 170, respectively) are reasonably similar. This suggests that the 60 °C, 85% RH stress test equitably evaluates the degradation time in the field for these two module designs. While not explicitly compared here, an accelerated stress test that uses a foil to ground the module face would uniformly degrade all three module designs and thus not be able to differentiate their anticipated rate of degradation in the field. We could not see any notable correlation in the coulombs accumulated in leakage current at the 5% relative power degradation mark. Electronic charge transfer appears here, as anticipated, not to serve as a direct indicator for forecasting the field performance.

Despite the frameless design not showing any clear degradation to date, it must be monitored further. It is conceivable that soiling on the module and mounting hardware over time may eventually produce leakage paths [15]. If significant leakage current pathways develop from the module face, across the back surface, across the fiberglass support rails, and to the ground mounting points, PID may eventually occur. While it is clear in this data that PID in the frameless module with rear mounting rails is superior in its PID resistance, its long-term durability must still be assessed.

3.3. Considerations for future developments in testing for system voltage durability

By performing the test at various labs and with various partners, further understanding of strengths, weaknesses, and areas for improvement in the testing protocol have been identified. Tests of the protocol with two module designs at five labs or research institutes have shown the ability of the test to satisfactorily differentiate the passing and failing module designs [24]. It is however understood that the rate of degradation is sensitive to variations in temperature and RH and the uniformity of these parameters in the chamber, and concerns have been raised about humidity on the module in excess of equilibrium just after a ramp in temperature. A startup sequence is being developed in a chamber with the ramp that does not leave excess humidity on the module surface, and requests have been made for extending time and temperature over the existing protocol specifications for a margin of safety.

Methods to evaluate PID using foil on the module surfaces have also been proposed, including at 25 °C [5,20] and at 70 °C [25]. The convenience of a 25 °C test can be envisioned; however, methods for achieving precise and repeatable contact are unclear, as is whether this temperature level significantly below what is seen in the natural environment with the module face covered by foil can correctly evaluate PID and polarization. The tests of the conventional framed module design that degraded 5% relative in power in approximately 11 h at the 60 °C, 85% RH condition (Figure 4) required approximately 390 h to degrade 5% with the 25 °C Al foil test (Figure 6). There is significant uncertainty in the time to 5% degradation in chamber because of the quick rate of degradation of this module, so further work is necessary to evaluate the ratio of acceleration between these tests.

Repli cas of this design also started failing at the 5% relative degradation point in the Florida outdoor tests in about 92 days (Figure 5, framed modules). It is clear that 390 h under such an Al foil test would not be anywhere near sufficient in duration to determine durability to PID on the basis that a PID-durable module should survive 96 h in the IEC 62804 draft protocol, and this design failed.

Figure 5. Degradation as a function of time for three module designs under −1000 V bias during daylight hours and control modules that are self-biased near the maximum power point with load resistors in the outdoor environment. The colors of the data points indicate the irradiance in the plane of array. Spline fits are shown for each of the three replicas of each module design their—their points and corresponding fitting curves are indicated in the bottom-right of the plot. Due to the influence of seasonality, the data is not fit with a time-squared abscissa here. I–V sweeps were not frequently collected during the early stages of the test due to late optimization of the algorithm for triggering on-sun I–V tracing. The start date of the test was the 28th of August, 2012.
in around 11 h. It is therefore likely that a module that degrades to a pass/fail cutoff of 5% at 25 °C under Al foil could take an inconveniently long time to yield durability information. Published durations for the 25 °C test, such as 168 h \[5,19\], appear insufficient, so further work is required to develop the relevant stress levels, durations, and understanding of the limitations for tests using foil conductors on the module faces.

It has been noted in the literature that the junction failure associated with PID in conventional cell modules leads to more extreme low-light performance degradation compared with that under STC \[26\]. Low-light performance is desired for energy yield. This understanding has led to the request for the testing of low-light performance in PID, or extending the duration of the stress test so that any degradation in low-light performance is captured later, after degradation continues to progress, by flash testing using 1000 W/m².

To quantify the trends in low-light performance compared with higher irradiance conditions, the degradation curves captured during the course of PID outdoors between 700 and 1000 W and between 200 and 350 W are normalized for one-sun equivalence and adjusted for temperature by the \(\gamma\) factor. The degradation in \(P_{\text{max}}\) for these two ranges is shown in Figure 7 for the two-edge frame design, for which the rate of degradation is easily visualized. These modules had good low-light performance in the new, unstressed state, where the normalized power for both the low-irradiance and

![Figure 6](image1)

**Figure 6.** Degradation of two replicas of potential-induced degradation-sensitive framed modules under \(-1000 \text{ V bias, 25 °C, 40% RH, module face grounded with Al foil weighted down by a rubber mat. The modules are seen to fail here at 5% relative degradation in 390 h. In comparison, a replica of this module degraded 5% relative by potential-induced degradation in about 92 days in the field (framed design in Figure 5).**

![Figure 7](image2)

**Figure 7.** Standard test conditions-adjusted power normalized to initial values at time zero for three two-edge framed modules mounted in Florida under \(-1000 \text{ V system voltage bias applied during the daytime. The abscissa represents the days (24 h cycles) that the modules have been in test. The points are taken from I-V sweeps with irradiance in the plane of array from 200–350 W/m² for the low-light condition and for the range 700–1000 W/m². We can observe the development of degraded low-light performance as potential-induced degradation progresses.**

<table>
<thead>
<tr>
<th>Design</th>
<th>Time to 0.95 (P_{\text{max0}})</th>
<th>Acceleration factor in time</th>
<th>Coulombs to 0.95 (P_{\text{max0}})</th>
<th>Acceleration factor in charge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Framed</td>
<td>92</td>
<td>0.46</td>
<td>200</td>
<td>0.856</td>
</tr>
<tr>
<td>2-edge framed</td>
<td>256</td>
<td>1.51</td>
<td>170</td>
<td>1.68</td>
</tr>
<tr>
<td>Rear rails</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
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<table>
<thead>
<tr>
<th>Time to 0.80 (P_{\text{max0}})</th>
<th>Acceleration factor in time</th>
<th>Coulombs to 0.80 (P_{\text{max0}})</th>
<th>Acceleration factor in charge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Framed</td>
<td>310</td>
<td>0.82</td>
<td>378</td>
</tr>
<tr>
<td>2-edge framed</td>
<td>*</td>
<td>2.83</td>
<td>*</td>
</tr>
<tr>
<td>Rear rails</td>
<td>*</td>
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The modules with the rear rails are not degraded at all, and the modules with the two-edge frame are not sufficiently degraded to evaluate the acceleration for the 0.80 · \(P_{\text{max0}}\) failure criterion at this writing.

*module not sufficiently degraded
high-irradiance regimes follow close to one another. The low-light curves shown in Figure 7 degraded to 0.95 fraction of the original power (from top to bottom) at 17%, 35%, and 42% less time than the full-light curves. Seasonality, whereby degradation slows or even reverses, can elongate the interval between the two curves. In comparison, another study showed the failure when measured at the low-light level occurs in 28% less time than that at full irradiance for the PID testing of mc-Si modules in the environmental chamber (60 °C, 85% RH) and –1000 V bias [27]. It appears on the basis of these results that the accelerated degradation in low-light performance may be accounted for by extending the test duration, as an alternative to physically measuring the degradation in low light at an earlier point in time.

Future work should include testing a variety of silicon module designs, including n-base cells and heterostructure cells that have commonalities with amorphous Si cell technologies, and understanding the longer-term effects of system voltage on Si-based cells. While the current IEC standard under development encompasses only c-Si cell modules in its scope, research toward the understanding of the needs of various thin-film technologies is also necessary to set appropriate stress levels for their qualification testing.

4. SUMMARY AND CONCLUSIONS

The 60 °C, 85% RH with system voltage stress condition proposed in the IEC 62804 Ed. 1 system voltage durability qualification test under development successfully differentiated the outdoor performance for framed and two-edge framed mc-Si PV modules. These two designs showed similar acceleration factors for time to 5% degradation, the pass/fail limit of the test. The two-edge frame module design that fail in 96 h have also proved to be unstable in the natural environment, whereas the modules with rear rails passes the test protocol and appear stable so far in the natural environment. Longer-duration testing of the module design with rear rails is however required. A grounded foil wrapping the module would short-circuit the benefits of these PID-resisting mounting designs that have already been frequently implemented for thin-film PV modules. A standard using foil that would prevent manufacturers from using a viable design to achieve PID resistance is a concern. The results showed that a 25 °C test with foil used to ground the module face could be prohibitively long in duration. We showed 28 month outdoor data for two module designs that provide the basis for the 5% degradation limit with 96 h at 60 °C, 85% RH system voltage stress that has been proposed to qualify modules for PID durability. Tests of modules with modified frames provide additional data supporting the proposed pass/fail criterion of the draft standard. Low-light module power performance was measured and compared with standard test conditions performance in outdoor PID testing. It was found that modules degraded 5% (relative) in the range of 17–42% less time when measuring at 200 than at 1000 W/m² irradiance. This range is attributed to the effects of seasonality.

ACKNOWLEDGEMENTS

The authors thank Bill Marion for helpful discussions; Steve Rummel and Allen Anderberg, Keith Emery, Showalter, Donard Metzger, and Stephen Barkasi for module measurements; and Antonio Bonucci for providing module edge tape. This work was supported by the US Department of Energy under Contract No. DE-AC36-08-G028308 with the National Renewable Energy Laboratory.

REFERENCES


